Recent advances in GaAs JFETs for deep cryogenic focal plane readouts

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ABSTRACT

The progress of the Jet Propulsion Laboratory in developing gallium arsenide junction field-effect transistors (GaAs JFETs) for application in infrared readout electronics operating below 10 Kelvin is discussed. Results on GaAs JFETs fabricated using a highly isotropic HF-based etchant have been presented previously by our group. The isotropic etch reduced the typical input leakage current at 4 K to less than 1 fA. These JFETs had a low frequency noise of just under 1 $\mu V/Hz^{1/2}$ at 1 Hz at 4 K, while dissipating less than 1 μW of power. Building on this work, we have fabricated small-scale integrated circuits based on this GaAs JFET technology. In this paper we report on the fabrication of small-scale integrated circuit multiplexers and amplifiers. An 8x1 source-follower-per-detector multiplexer and a three-transistor differential pair have been fabricated and are fully functional at 4 K. The input-referred noise and leakage current is consistent with that for the discrete devices. A systematic study of the device size dependence of the noise has been started, but as yet is inconclusive.

Keywords: GaAs, JFET, multiplexer, cryogenic, low temperature, infrared detectors, readout, noise.

1. INTRODUCTION

Future ground-based, space-based, and balloon-borne telescopes for infrared astronomy will employ detectors cooled to deep cryogenic temperatures (below 10 K). This includes photovoltaic and photoconductive detectors for the very long wavelength infrared (VLWIR) (approximately 50 μm to 200 μm wavelength), as well as bolometers for 100 μm to millimeter-wave radiation. For small arrays of such detectors consisting of less than ten pixels or so, it previously had been adequate to cool only the detector array to deep cryogenic temperatures, and to run a wire from each pixel to a warmer compartment containing the readout electronics. These wires carry heat to the cold head, however, and they are susceptible to noise pickup, which makes this approach impractical for larger arrays or for ultra-low noise levels envisioned for future IR instruments.

Therefore, several different groups have been exploring readout electronics that can operate at 10 K and below, and that can be placed on the cold head immediately adjacent to the detector array[1-6]. Clearly such electronics must circumvent carrier freeze-out and be functional below 10 K. They must also dissipate low power, and have low noise and low input current. Typically the power dissipation must be at most a few microwatts per channel. Photoconductive and photovoltaic detectors usually require input leakage currents of a few hundred electrons per second and noise values of less than 1 $\mu V/Hz^{1/2}$ at 1 Hz. Bolometer readout applications usually are less restrictive on the leakage current but more demanding on noise, requiring input impedances hundreds of megaohms and input-referred noise voltages as low as 10 $nV/Hz^{1/2}$.

JPL has been exploring GaAs JFET-based electronics for such applications for the past several years[7]. Because of the very small electron effective mass in GaAs, moderately doped n-type GaAs can be made immune to carrier freeze-out, and a p+ on n JFET can be made that will operate normally from room temperature down to 4 K. We have concentrated on JFETs rather than MESFETs because the higher gate barrier provided by the p-n junction in the JFET usually results in the JFET having less gate leakage current than a MESFET. The principal challenge for our effort has been to reduce the noise and gate leakage current to acceptable levels.

By using a highly isotropic HF-based etchant[8], JPL has been able to fabricate discrete GaAs JFETs with input leakage currents of less than 1 fA at 4 K, and with input-referred noise values of less than 1 $\mu V/Hz^{1/2}$ at 1 Hz when dissipating less than 1 μW of power[9]. We have now progressed to small-scale integrated circuit readout amplifiers and multiplexers, based on this GaAs JFET technology. In the remainder of the paper, we discuss the basics of the JFET fabrication, the design of the multiplexers and amplifiers, and our plan for exploring and reducing the device noise.

2. THE DEVICE STRUCTURE

The JFET structure is shown in Fig. 1. Starting on a semi-insulating GaAs substrate, MBE is used to grow an undoped buffer approximately 1 μm thick, followed by an n-type channel several hundred nanometers thick, capped with a p+ junction layer 50 nm thick. The channel is doped with silicon to a range of 10^{16} to 10^{17} cm^{-3}. After growth, the p-layer is etched back to expose the n-layer for source and drain contacts, and the transistor mesas are defined by etching down to the substrate. The ohmic contacts to the source and drain are made using an alloyed Ni/Ge/Au metallization. Contact to the heavily doped p-type gate layer is made using a non-alloyed Ti/Pt/Au metallization.

A highly isotropic HF-based etchant was used to make the etching sidewalls as smooth as possible, in order to avoid sharp edges that could increase the leakage current through electric field concentration. The details of the fabrication, including the wet chemical etching, have been previously published[7,9].

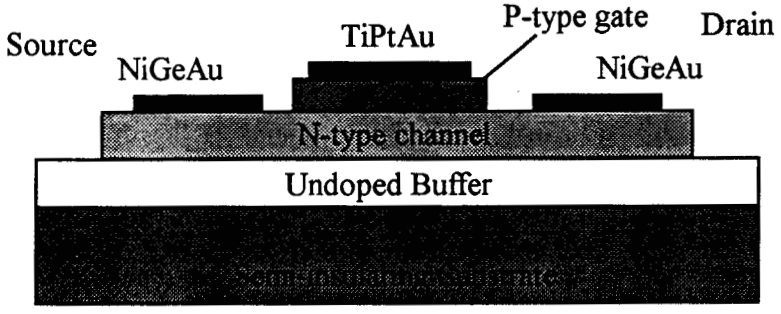

Fig. 1: The structure of the GaAs JFET produced by MBE growth and etch-back. The undoped buffer is approximately 1 μm thick. The n-type channel is 3750 Å thick and doped with silicon to 5×10^{16} cm^{-3}. The p-type gate is 500 Å thick and is doped to greater than 5×10^{18} cm^{-3}.

3. MULTIPLEXER AND AMPLIFIER FABRICATION

Having demonstrated reasonable performance in discrete GaAs JFETs, we began the task of fabricating small-scale integrated circuit amplifiers. The basic device fabrication was the same as for the discrete JFETs, with the addition of a dielectric layer and an interconnect metallization. First, the individual JFETs were made using the gate etch, ohmic contact metallization, device isolation etch and gate metallization, as described previously. Then, polyimide was spun on and cured. The contact openings were opened in the polyimide layer by reactive ion etching in an oxygen plasma, using a photoresist mask. Then, the contact metallization consisting of 20 nm of chromium under 200 nm of gold was deposited and patterned using lift-off. The pads for wire bonding were also formed from this metallization.

An 8x1 source-follower-per-detector multiplexer was fabricated by this method. An abbreviated schematic showing the common circuitry and two of the eight cells of the array is shown in Fig. 2. In actual operation, a VLWIR photodiode from an array would be connected to each of the input nodes.

A simple differential pair was also included on the mask set with the multiplexer. It consists of a pair of JFETs with separate gate and drain contacts. The sources of the JFETs are joined and connected to a common current load JFET. This differential pair is also shown in Fig. 2.

Each cell of the multiplexer contains three GaAs JFETs: one configured as a source-follower buffer, the second used as a reset switch, and the third used as a select switch. When the reset JFET is on, it connects the cell's input to the common V_{Reset} line, resetting the input. In actual operation this would also set the bias on the VLWIR photodiode connected to the input. When the JFET reset switches are opened, and the inputs of the cells are isolated.

To select a particular cell for readout, the individual select line for that cell is brought high, turning on the JFET select switch for that cell. That connects the source of the source-follower JFET in the cell to common current source, through the common output bus. The cell's source-follower JFET then drives the output bus at a voltage equal to the cell's input, plus a fixed offset voltage. As the input voltage changes (as would be the case if a photodiode connected to the input was collecting optical signal), the output voltage is driven to follow it.

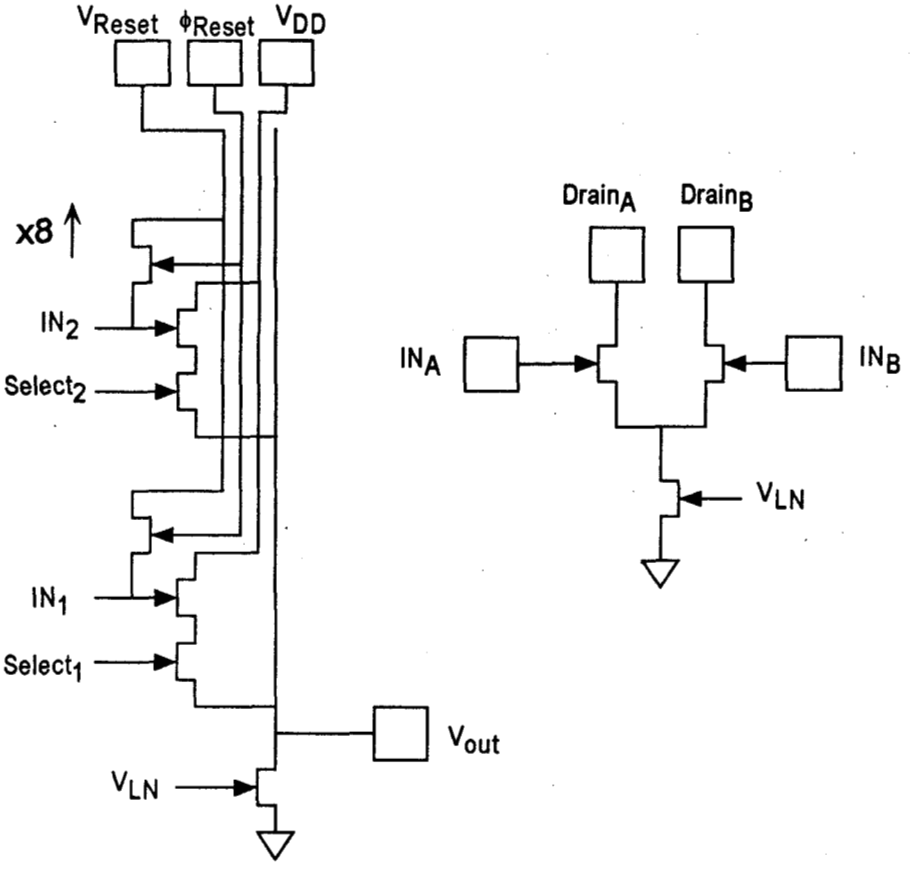

Fig. 2: The schematics of small-scale integrated circuits made from GaAs JFETs. Shown on the left is part of an 8×1 multiplexer. Two of the eight cells are shown, along with the common current-source load transistor and the column lines and pads. Shown on the right is a simple differential pair including a common current load transistor.

4. MULTIPLEXER NOISE AT 4 K

The multiplexer shown in Fig. 2 was tested at 4 K using an external biased at a current of 50 μA. The input was biased by pulsing ϕ_{Reset} high with a voltage on V_{Reset}, then isolated by returning ϕ_{Reset} low. The output voltage noise with the input isolated was recorded using an HP3561 dynamic signal analyzer and a PAR113 preamplifier. Typical noise performance is shown in Fig. 3.

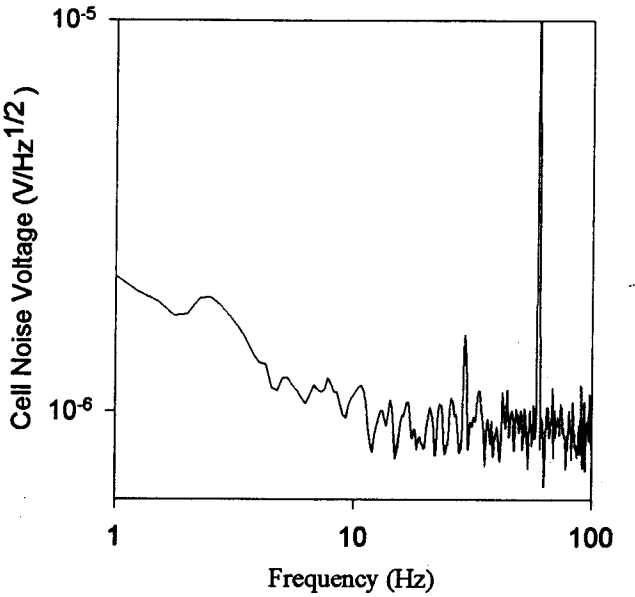

Fig. 3: The output noise voltage from one cell of the 8x1 multiplexer at 4 K with the input floating and isolated. The source-follower was biased with an external current source of 50 μA, and the measured source-follower gain was 0.88. The noise spike at 60 Hz is line frequency pickup.

5. SYSTEMATIC NOISE STUDIES ON DISCRETE DEVICES

In order to better characterize the noise, we have fabricated discrete JFETs ranging in size from 20 μm × 10 μm to 500 μm × 500 μm. A table listing the size of these JFETs is shown in Table 1. We have also fabricated multiple versions of JFETs of the same size. We are now measuring the noise performance of these discrete JFETs at 4 K in order to determine whether there is a systematic dependence of the noise on the device perimeter or area. This study is not yet complete, but preliminary results indicate that the random device to device variation, even among devices of the same size, is at this time larger than any systematic size dependence of the noise.

Label	Width (μm)	Length (μm)
A	1250	50
B	625	50
C	315	50
D	10	500
E	100	400
F	90	200
G	45	200
H	45	100

Label	Width (μm)	Length (μm)
I	25	200
J	25	100
K	25	50
L	500	10
M	100	10
N	50	10
O	20	10
P	20	20

Label	Width (μm)	Length (μm)
Q	100	20
R	500	500
S	20	50
T	50	500
U	50	100
V	50	50

Table 1: The sizes of the GaAs JFETs on a single chip, used to study the size dependence of the noise and other parameters. JFETs A, B, and C are ring structure FETs: the width is the circumference of the ring gate and the length is the thickness of the ring. All of the other JFETs are rectangular.

6. SUMMARY

In summary, we had previously demonstrated GaAs JFETs functional at 4 K, and by employing an isotropic HF-based etchant we had reduced the input leakage current to less than 1 fA. This leakage is low enough for nearly all bolometer applications and is approaching the value needed for photovoltaic detector readouts, although it is still somewhat high for typical applications. Using this GaAs JFET technology, we have fabricated and tested prototype readout circuits at 4 K. The output noise from a cell of an 8x1 multiplexer at 4 K with a 50 μA bias and with the input isolated was just over 1 $\mu V/Hz^{1/2}$ at 1 Hz. This noise is low enough for the readout of some photoconductive and photovoltaic detectors, but at least an order of magnitude too high for bolometer readouts. We are now focussing on reducing this noise voltage. A set of JFETs of widely different sizes has been fabricated to help characterize the noise, but so far any systematic size dependence is masked by the larger device to device variation.

7. ACKNOWLEDGMENTS

The research described in this paper was performed by the Center for Space Microelectronics Technology, Jet Propulsion Laboratory, California Institute of Technology, and was sponsored by the National Aeronautics and Space Administration, Office of Space Science.

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